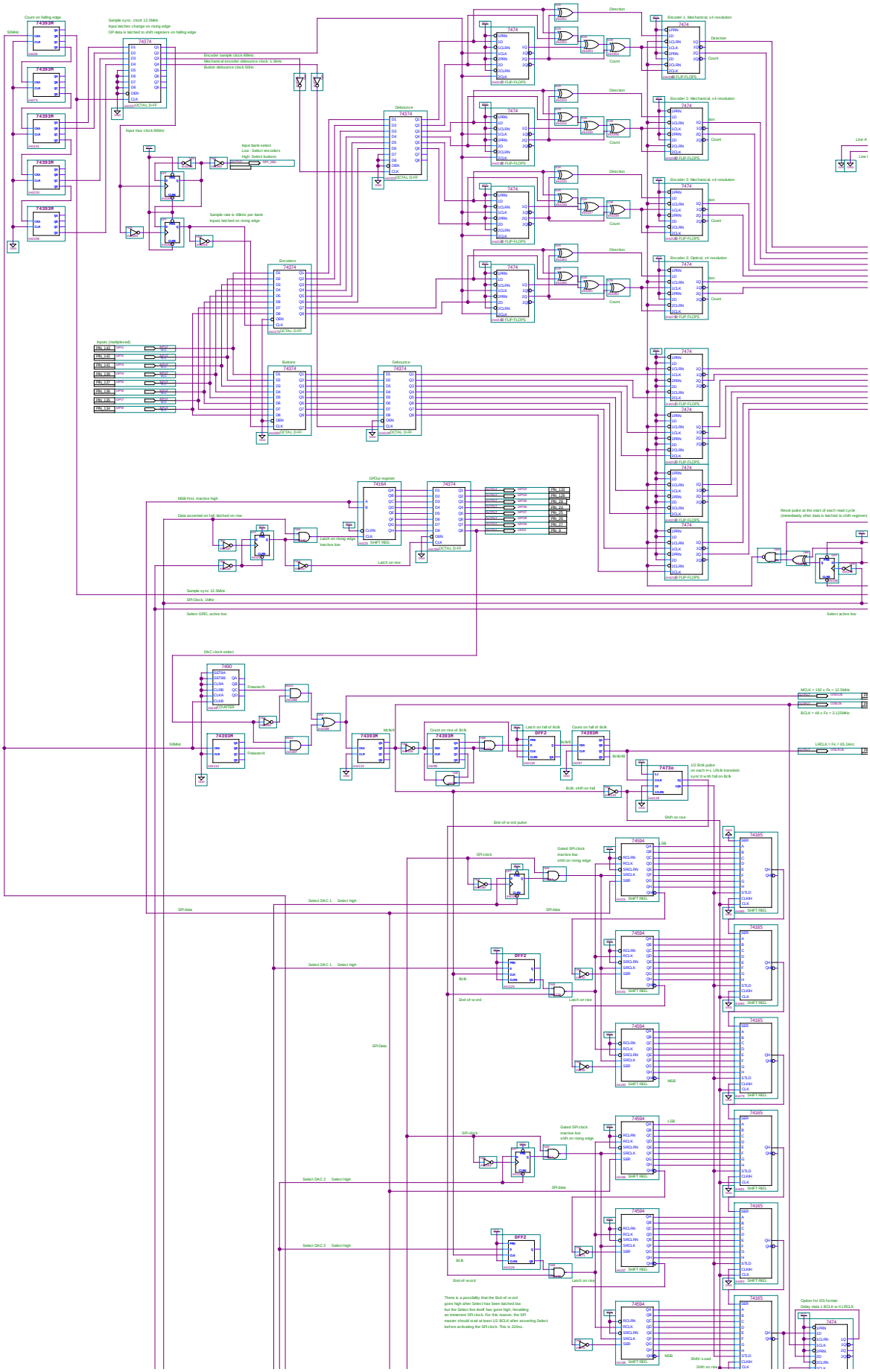
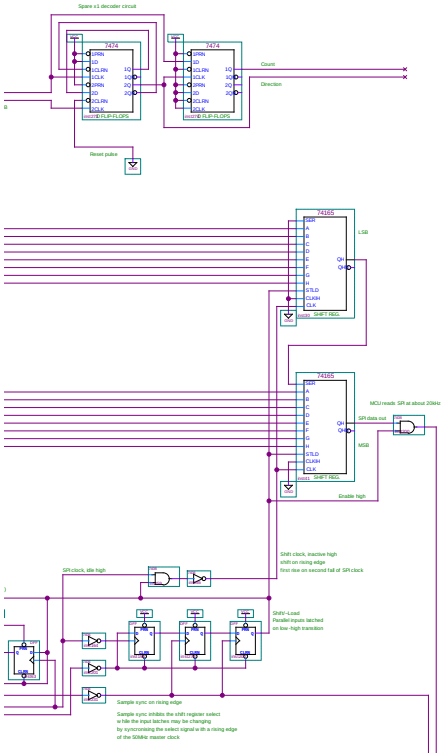
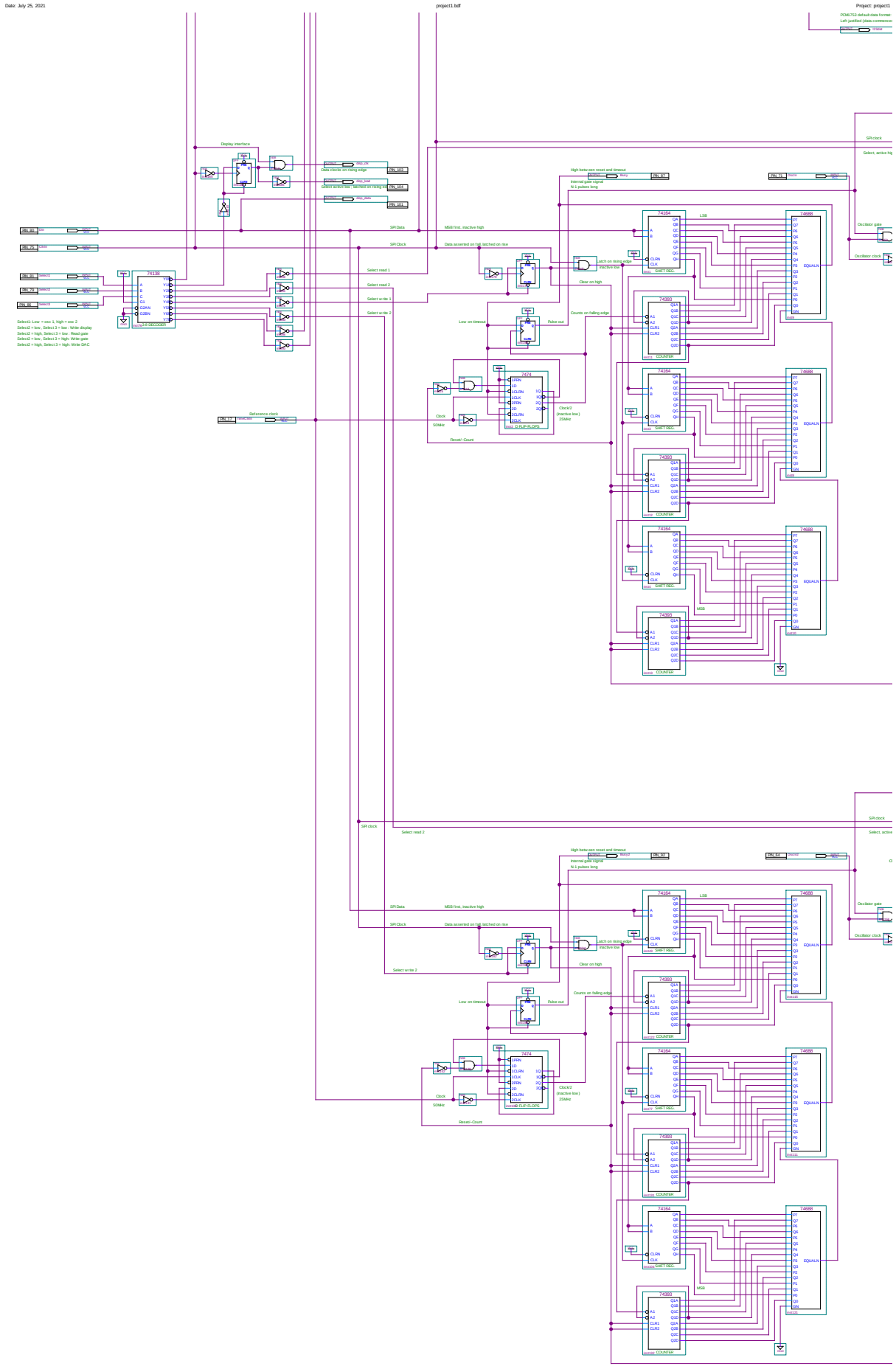
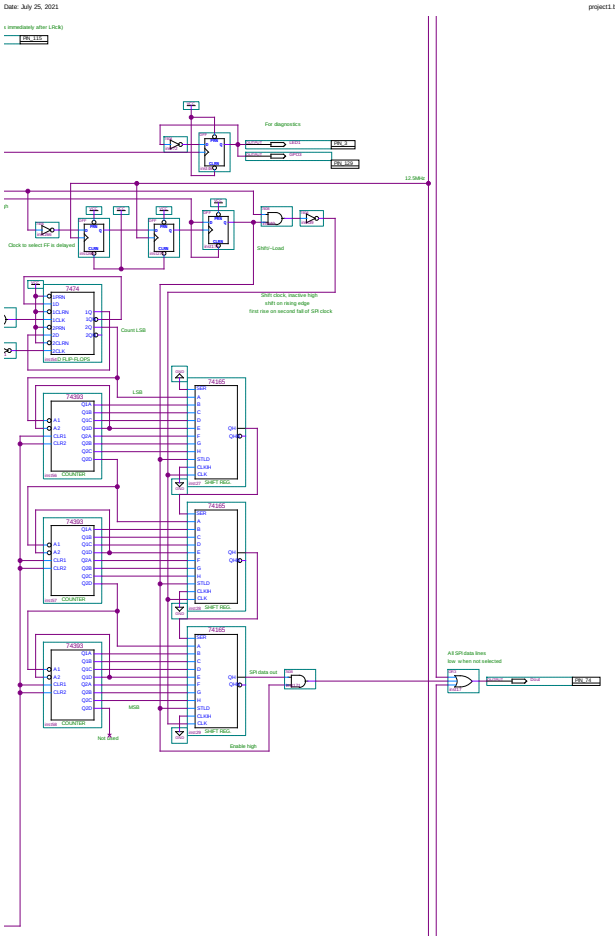
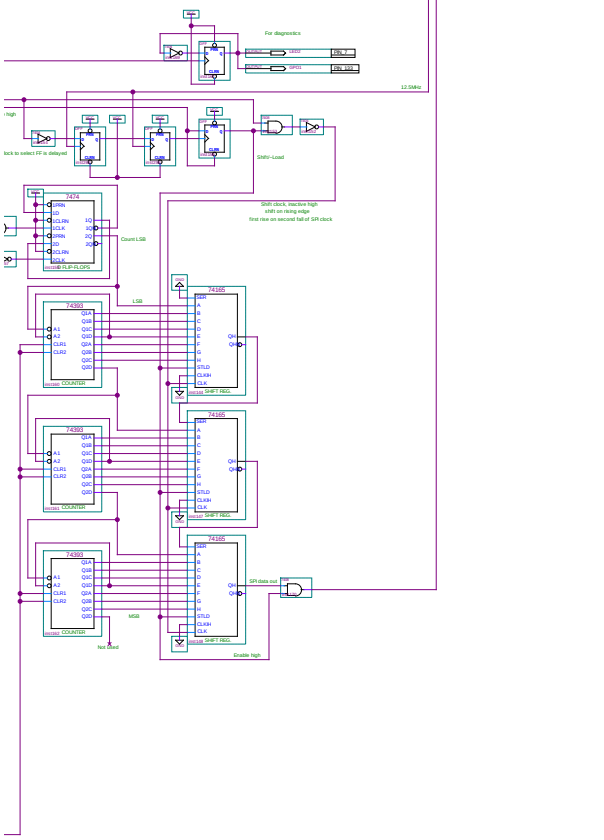

Count on falling edge
50MHz
74393N
Sample sync: clock 12.5MHz
Input latches change on rising edge
O/P data is latched to shift registers on falling edge
74374
OCTAL D-FF
Encoder sample clock 48kHz
Mechanical encoder debounce clock: 1.5kHz
Button debounce clock 50Hz
Input max clock 96kHz
Input bank select
Low : Select encoders
High: Select buttons
Sample rate is 48kHz per bank
Inputs latched on rising edge
Debounce
Encoders
Buttons
Inputs (multiplexed)
Direction
Count
Encoder 1: Mechanical, x4 resolution
Encoder 2: Mechanical, x4 resolution
Encoder 3: Optical, x4 resolution
7474
D FLIP-FLOPS
Line A
GPOut register
74194
SHIFT REG.
MSB first, inactive high
Data asserted on fall, latched on rise
Latch on rising edge
inactive low
Latch on rise
Reset pulse at the start of each read cycle
(immediately after data is latched to shift registers)
Sample sync 12.5MHz
SPI Clock, 1MHz
Select GPIO, active low
Select active low
DAC clock select
7490
COUNTER
Freq/256
Freq/64
50MHz
74393N
MclkN
Count on rise of Bclk
Latch on fall of Bclk
Count on fall of Bclk
Bclk/4
Bclk/48
74373o
1/2 Bclk pulse
on each H-L Lrlck transition
sync'd w ith fall on Bclk
Bclk: shift on fall
Shift on rise
MCLK = 192 x Fs = 12.5MHz
BCLK = 48 x Fs = 3.125MHz
LRCLK = Fs = 65.1kHz
End-of-word pulse
SPI clock
Gated SPI clock
inactive low
shift on rising edge
SPI data
Select DAC 1 Select high
Select DAC 2 Select high
Bclk
End-of-word
Latch on rise
SPI Data
MSB
LSB
74594
SHIFT REG.
74165
SHIFT REG.
DFF2
There is a possibility that the End-of-w ord
goes high after Select has been latched low
but the Select line itself has gone high, heralding
an imminent SPI clock. For this reason, the SPI
master should w ait at least 1/2 BCLK after asserting Select
before activating the SPI clock. This is 320ns.
Shift/~Load
Option for I2S format:
Delay data 1 BCLK w rt LRCLK


Spare x1 decoder circuit
7474
SPRN
LD
CLRN
CLK
SPRN
D
DCLRN
DCLK
1Q
1Q
2Q
2Q
D FLIP-FLOPS
Reset pulse
Count
Direction
74165
SHIFT REG.
LSB
MCU reads SR at about 20kHz
SPI data out
MSB
Enable high
SPI clock, idle high
Shift clock, inactive high
shift on rising edge
first rise on second fall of SPI clock
Shift-Load
Parallel inputs latched
on low-high transition
Sample sync on rising edge
Sample sync inhibits the shift register select
while the input latches may be changing
by synchronising the select signal with a rising edge
of the 50kHz master clock


PCM1753 default data format:
Left justified (data commences
Display interface
Data clocks on rising edge
Select active low - latched on rising e
SPI clock
Select, active hig
High betw een reset and timeout
Internal gate signal
N-1 pulses long
PIN_87
PIN_71
Oscillator gate
Oscillator clock
PIN_30
PIN_26
PIN_21
PIN_79
PIN_35
PIN_27
SPI Data
SPI Clock
MSB first, inactive high
Data asserted on fall, latched on rise
Select read 1
Select read 2
Select write 1
Select write 2
74138
Select0: Low = osc 1, high = osc 2
Select2 = low , Select 3 = low : Write display
Select2 = high, Select 3 = low : Read gate
Select2 = low , Select 3 = high: Write gate
Select2 = high, Select 3 = high: Write DAC
Reference clock
Latch on rising edge
Inactive low
Clear on high
Pulse out
Low on timeout
Counts on falling edge
74164
LSB
SHIFT REG.
74688
EQUAL(N)
74393
COUNTER
MSB
7474
D FLIP-FLOPS
Clock
50MHz
Clock/2
(inactive low )
25MHz
Reset/~Count
SPI clock
Select, active
Select read 2
High betw een reset and timeout
Internal gate signal
N-1 pulses long
PIN_82
PIN_84
SPI Data
SPI Clock
MSB first, inactive high
Data asserted on fall, latched on rise
Select w rite 2
Latch on rising edge
Inactive low
Clear on high
Pulse out
Low on timeout
Counts on falling edge
74164
LSB
SHIFT REG.
74688
EQUAL(N)
74393
COUNTER
MSB
7474
D FLIP-FLOPS
Clock
50MHz
Clock/2
(inactive low )
25MHz
Reset/~Count
Oscillator gate
Oscillator clock


For diagnostics
12.5MHz
Clock to select FF is delayed
Shift/~Load
Shift clock, inactive high
shift on rising edge
first rise on second fall of SR clock
7474
Count LSB
LSB
MSB
Not used
Enable high
SR data out
All SR data lines
low when not selected


For diagnostics
12.5MHz
Shift/~Load
Shift clock, inactive high
shift on rising edge
first rise on second fall of SR clock
7474
Count LSB
LSB
MSB
Not used
Enable high
SR data out